Recent Progress of Submicron CMOS Using 6H–SiC for Smart Power Applications

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***Abstract*— Silicon carbide (SiC) CMOS circuits have been developed recently to provide monolithic control for SiC MOS power switching devices. Although SiC CMOS is not well suited for high-end microprocessor applications, it must provide the necessary response time performance required for safe operation in high-voltage power switching applications. Despite previous developments in SiC CMOS process technology, which have enabled digital circuit operation using a 5 V power supply, circuit switching speeds were in the microsecond range. An obvious way to improve circuit performance is to scale device lateral and vertical dimensions. This paper describes recent progress in the development of a submicron, single metal, p-well CMOS process technology using 6H-SiC. Conventional NMOS transistors are fabricated with 0.5-mm (drawn) channel lengths and exhibit acceptable short-channel effects. Conventional PMOS transistors exhibit punchthrough at 0.8-mm channel lengths and require considerable channel engineering efforts which are also presented. Several digital logic gates and a ring oscillator have been fabricated with nanosecond gate switching performance. Performance limiting factors like parasitic series resistance is also investigated.**

***Index Terms*—High-temperature, MOSFET's, silicon carbide.**

I. Introduction

THE advantage of complementary technologies is the availability of current source loads which provide large voltage gains with relatively small supply voltages and currents. Advances in SiC process technology have led to the development of CMOS circuits. The first complementary device technology using 6H-SiC enhancement-mode MOSFET's demonstrated a functional operational amplifier with a DC gain of about 10^4 (80 db) [1]. However, the threshold voltage for the p-channel devices fabricated in an implanted n-well was around -17 V. The high threshold voltage requires a large power supply voltage which is incompatible with the conventional CMOS digital logic. Recently, an implanted p-well CMOS process has been successfully developed to fabricate digital circuits using a lower supply voltage [2]. The threshold voltage for the NMOS and PMOS devices were 3 and -8 V, respectively. In [3], the authors demonstrate SiC CMOS logic circuits operating on a 5 V power supply. The lower supply voltage reduces the stress on the thermal oxide, and thus provides the greatest opportunity for reliable circuit operation.

CMOS and most power MOS transistors (DIMOS and lateral DMOSFET [4], [5]) in SiC were developed using boron implantation to form a p-well in an n-type SiC epilayer. The compatibility of their processes eases integration of the power device and CMOS digital control circuits on the same SiC wafer to from a smart power IC. Because SiC power switching devices operate at high-current and high-power levels, self-heating is expected to cause device junction temperatures to exceed 350 °C. Therefore, the circuits implmenting the support electronics on a smart power chip must provide reliable and stable operation over a wide range of temperatures. Because of its wide bandgap, SiC NMOS and CMOS circuits have demonstrated stable operation ranging from room temperature to 300 °C [3], [6].

Smart power technology usually combines detection circuitry together with digital and analog feedback control to protect the IC from catastrophic failure. CMOS operational amplifiers and intelligent gate drivers that provide stable operation at elevated temperatures have already been performed on SiC [7], [8]. As a robust smart power system becomes more complex, CMOS circuits are required to have higher performance and higher density in order to provide the control, diagnostic, and self-protection functions. The response time of these circuits is critical to a benign shutdown because the power load current will increase very abruptly during an over-current or over-voltage fault. For medium-frequency applications such as adjustable speed motor drives, turn-off times of power device range from 0.1 to 10 μs [9]. The turn-off time of SiC power switching device in the range of 0.1 μs has already been demonstrated in [10]. As the high-speed operation of power devices is required, the protection of the system can only be accomplished by utilizing suitably fast control circuits to provide the necessary response. However, current CMOS digital logic circuits can only operate with a gate delay per stage of 442 μs with a VDD of 5 V, and 0.45 μs for a VDD of 20 V. With this technology, even a single inverter stage is incapable of turning off a power system in a rapid response time. Scaling of device dimensions is the main force of increasing circuit speeds. This critical issue has led to the development of a submicron CMOS technology in 6H-SiC capable of providing the performance suited for smart power applications.

In this paper, a submicron CMOS technology with sub-0.1-μs gate delays was developed aiming at the smart power application. For this study, CMOS devices in 6H-SiC are

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fabricated in the 0.5-μm region. The NMOS transistors in the p-well are conventional while the PMOS transistors require a channel implant to suppress source-drain punchthrough. Device electrical characteristics are measured and discussed. Digital logic circuits have been implemented and show a significant improvement over those described in earlier works [3].

II. Device Fabrication

CMOS devices are fabricated on a 10-μm thick, lightly doped n-type 6H-SiC epilayer with doping of 5×10^{15} cm^{-3} grown on a heavily doped n$^+$ substrate. Boron is implanted at 650 °C using a Ti/Au mask to form a 1-μm deep retrograde p-well in the n-epilayer. The profile is obtained using a multiple implantation with energy/dose rates of 20 keV/4.5 e 12 cm^{-2}, 45 keV/7.5 e 12 cm^{-2}, 85 keV/1.1 e 13 cm^{-2}, 140 keV/1.7 e 13 cm^{-2}, 230 keV/3.0 e 13 cm^{-2}, and 380 keV/1.8 e 14 cm^{-2}. The wafer is then selectively implanted with nitrogen (40 keV/2.5 e 15 cm^{-2}, 90 keV/3.0 e 15 cm^{-2}, and 160 keV/5.0 e 15 cm^{-2}) and aluminum (45 keV/2.2 e 14 cm^{-2}, 90 keV/3.4 e 14 cm^{-2}, 160 keV/5.4 e 14 cm^{-2}, and 270 keV/1.1 e 15 cm^{-2}) to form 0.25- and 0.3-μm deep source-drain regions for the NMOS and the PMOS transistors, respectively. The p$^+$ and n$^+$ regions are also used as channel stops for devices of opposite polarity. All implanted ions are activated at 1550 °C for 40 min in an Ar ambient.

The implant masks for submicron gate lengths are obtained by a combination of optical and electron beam lithography. Scaling MOSFET gate dimensions is the most obvious way to achieve higher performance. To this end, the device channel is defined by e-beam lithography while the remaining levels are patterned by optical projection. Previously [3], the overlap between the poly- silicon gate and the source/drain was the primary cause of the slow circuit speeds. In this process, the overlap is significantly reduced by accurate alignment via the e-beam lithography system.

The PMOS transistors are fabricated in the very lightly doped n-epilayer. A MEDICI simulation has revealed that punchthrough occurs when the p-channel gate length is scaled to less than 0.8 μm. To suppress the punchthrough current, simply increasing the substrate doping level is not appropriate because this will increase the threshold voltage and produce undesirable body effect. These undesirable effects can be eliminated using a deep nitrogen implant in the punchthrough region. In addition, boron is implanted in the surface to adjust the threshold voltage. The resulting implant profile is shown in Fig. 1. For a 0.8-μm PMOS, a substrate doping of 5×10^{16} cm^{-3} would be sufficient to prevent punchthrough. However, for 0.5-μm and smaller devices, a higher substrate doping is necessary and this may affect the threshold voltage for long-channel devices. The high-dose implant will also contribute to the body effect. The test wafer contains PMOS transistors of different channel lengths and a high implant dose for nitrogen was chosen to suppress the punchthrough for the smallest device. An optimized implant profile is required to trade-off the threshold voltage, punchthrough and body effect to fabricate PMOS transistors of varying sizes.

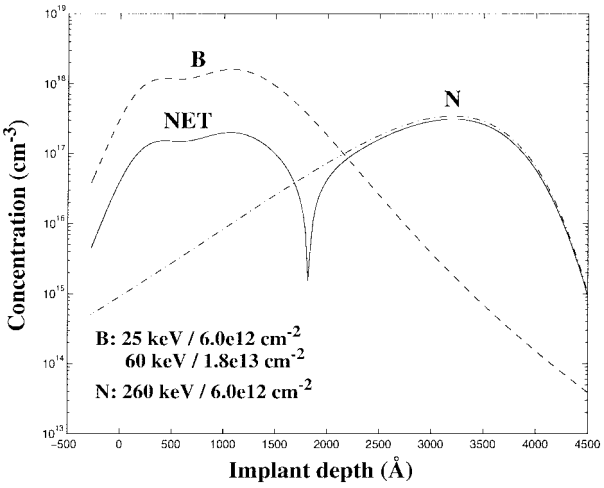


Fig. 1. A simulated implant profile in the p-channel region used as the punchthrough stopper and threshold adjustment.

After implant activation, a sacrificial oxide is grown and then stripped to remove the damage on the surface created by the implant anneal. The gate oxide is grown at 1150 °C for 1 h in wet O_2 and subsequently annealed in Ar for 30 min. A 5000 Å thick polysilicon layer is deposited by LPCVD and then doped to p-type by boron spin-on-diffusion. The polysilicon gate and the first interconnect layer are defined using a SF6 plasma etch. A 400 Å thick Al layer and a 200 Å thick Ni layer are deposited by lift-off process to form contacts on the p$^+$ and n$^+$ regions, respectively. All contacts are alloyed at 850 °C for 5 min in a RTA system. The wafer is then covered by plasma deposited silicon nitride as an interlayer dielectric. A contact hole etch is performed using a buffered oxide etch to provide access to the device contacts. To complete the fabrication, Al is deposited and patterned to form the interconnection.

III. Experimental Results

A. MOSFET Characteristics

High frequency photo-CV measurements at room temperature were performed on the MOS capacitors using an HP-4274 LCR bridge as described in [14]. The gate voltage was swept back and forth from accumulation to deep depletion in darkness except that the light was turned on at a bias point in deep depletion to generate photo-carriers. The gate oxide thickness obtained is 272 Å. The interface state densities and fixed charge densities calculated from the hook and ledge in the C–V curve measured on n-epilayer are in the range of 1.1–4.2×10^{11} eV^{-1} cm^{-2} and 1.0–3.0×10^{12} cm^{-2}, respectively. Photo-CV measurements of MOS capacitors fabricated on the p-well show a frequency dependence from 400 to 100 kHz. This is caused by the highly resistive B- implanted p-well. To take the series resistance into account, a quasi-static CV technique was used to extract the p-well doping. The equivalent frequency for the measurement is 0.25 Hz. The postanneal doping concentration is about 1.3×10^{17} cm^{-3}, which corresponds to an activation rate of 13%.

TLM structures were used to measure the sheet resistance of the heavily doped N and Al regions. Alloyed contacts to both

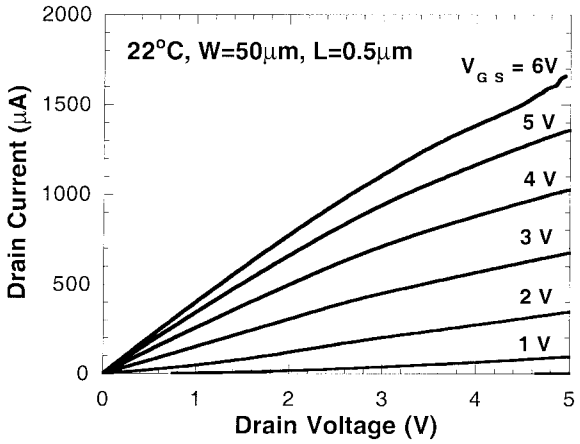


Fig. 2. $I-V$ characteristic of a NMOSFET with 0.5-μm channel length at room temperature.

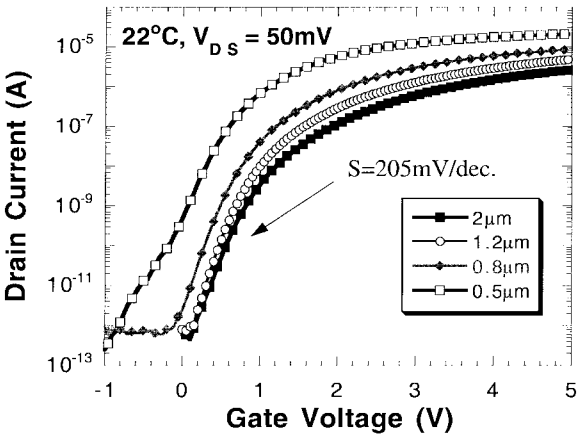


Fig. 3. Subthreshold characteristics of NMOS transistors with various channel lengths.

n^+ and p^+ regions are ohmic at room temperature. The n^+ region has a sheet resistivity, ρ_s, and specific contact resistivity, ρ_c, of 3.1 kW/sq and $1.65\times10^{-4}\ \Omega\ \text{cm}^2$, respectively. The ρ_s and ρ_c for the p^+ regions is 67 kΩ/sq and $6.7\times10^{-2}\ \Omega$-cm^2, respectively. The sheet resistivities of n^+ and p^+ layers are higher than the typical values reported in the literature [15], [16]. The high sheet resistance arises from the thin implanted layer used to form the source and drain for the short-channel device. A thickness of about 0.25–0.3 μm was targeted but because the oxidation rate on the heavily doped region is two to three times higher than that on the epilayer, a significant portion of the heavily doped implanted layer was consumed which caused the sheet resistance to increase.

The device characteristics for a 0.5-μm NMOS transistor is shown in Fig. 2. The saturated transconductance is 2.68 mS/mm and the threshold voltage extrapolated from the linear region of the I_d-V_g curve is 1.2 V. This device shows little saturation in drain current because of channel length modulation and drain-induced barrier lowering (DIBL). The I_d-V_g curve shows a shift of 0.95 V in threshold voltage as the drain bias is changed from 50 mV to 5 V. For a 0.8-μm device, the corresponding threshold voltage shift is only 0.3 V and the saturation characteristic in drain current is obtained. Parasitic resistances and effective channel lengths are extracted using the techniques described in [11], [12]. The device parasitic source-drain resistance, $R_{\rm SD}$, is $8.4\times10^3\ \Omega$-μm and $\Delta L(=L_{\rm drawn}-L_{\rm eff})$ is 0.26 μm. The subthreshold characteristics for different channel lengths are shown in Fig. 3 where subthreshold slopes of 205 mV/decade are obtained for long-channel devices. The channel mobility, extracted from $L_{\rm drawn}=5$- and 10- μm devices by subtracting their total resistance $R_T=V_D/I_D$ measured at $V_{\rm DS}=50$ mV, is 8.0–10.5 cm^2/V-s at room temperature.

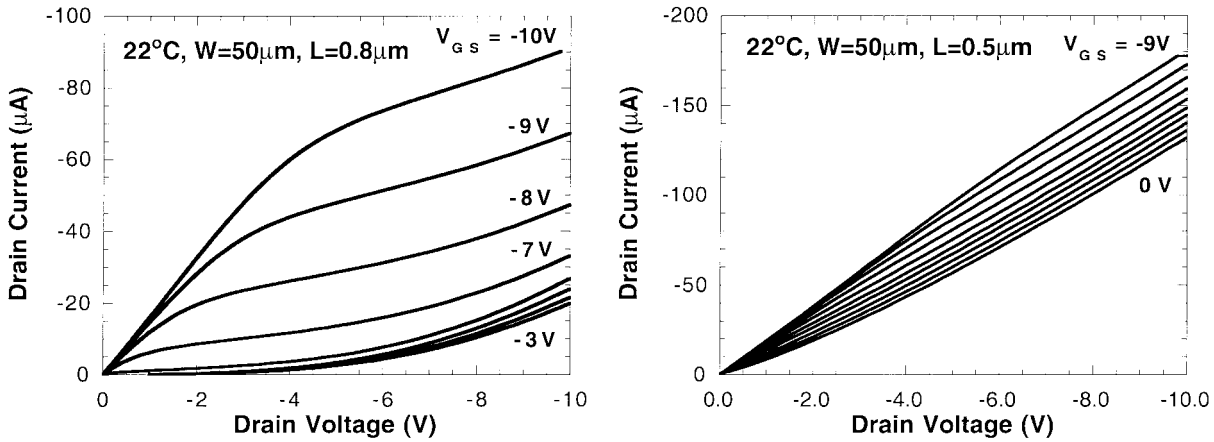
Fig. 4(a) shows the $I-V$ characteristic of an $L_{\rm drawn}=0.8\ \mu$m PMOSFET which does not have the anti-punchthrough implant in the channel. The leakage current at a low gate voltage and high drain bias indicates that punchthrough occurs as the sub-surface current spreads into the substrate rendering the gate ineffective. The threshold voltage and saturated transconductance for this device is -4.2 V and 0.32 mS/mm. $R_{\rm SD}$ and ΔL is extracted to be $3.5\times10^6\ \Omega$-μm and 0.28 μm, respectively. The 0.8-μm device displays adequate saturation characteristics while the 0.5-μm device displays resistance-like behavior, showing negligible gate control, as shown in Fig. 4(b). The subthreshold currents for PMOS transistors with various channel lengths shown in Fig. 5 indicate a poor subthreshold slope for the 0.8-μm device. The complete cutoff of the drain-to-source conduction for the 0.5-μm device cannot be achieved due to the punchthrough. The mobility measured from long-channel devices is 4.7 cm^2/V-s.

To suppress punchthrough, the substrate doping is increased by a very shallow nitrogen implant using the profile shown in Fig. 1. In this implantation, a high boron dose is used with its low activation rate taken into account to reduce the threshold voltage. The threshold adjustment was targeted at shifting the threshold 3 V toward zero. However, part of the implanted layer was removed during oxidation and this reduction could only be approximated. Relatively decent saturation characteristics are obtained for the 0.8- and 0.5-μm PMOS as shown in Fig. 6. The subthreshold slopes are also improved for the short-channel devices in Fig. 7. The implanted p-channel surface is p-type but the $I-V$ characteristics indicate that the device is a normally-off or enhancement mode device. This reveals that the p-type surface is depleted at a zero gate bias. The mobility for the long-channel device is about 2.0 cm^2/V-s.

It should be noted that the threshold voltage decreases with the channel length due to the short-channel effect. Fig. 8 shows the threshold voltage roll-off characteristics for NMOS and PMOS transistors. The V_T difference from long-channel to short-channel devices varies from 1.4 to 1.65 V. The deep nitrogen implant in the p-channel has increased the threshold voltage by 1.5 V for long-channel devices. The boron dose for the threshold adjust implant can be increased to shift threshold voltages to a more desirable value.

B. Circuit Results

Results of CMOS digital circuits using the single metal process are described in this section. Fig. 9(a) shows the inverter transfer characteristics for supply voltages ranging from 2 to 9 V. The PMOS channel is 30 μm wide and



(a) (b)

Fig. 4. Shown are the $I-V$ characteristics of (a) 0.8-μm and (b) 0.5-μm PMOS transistors without punchthrough stopper at room temperature.

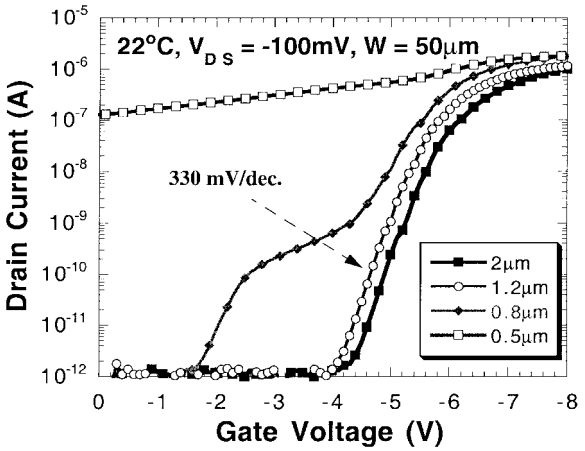


Fig. 5. Subthreshold characteristics of PMOS transistors without punchthrough stopper.

0.8 μm long-while the NMOS channel is 10 μm wide and 0.8 μm long. All PMOS devices in circuits do not have the anti-punchthrough implant. For normal CMOS operation, both PMOS and NMOS operate in enhancement mode and the sum of the magnitudes of threshold voltages for both transistors is less than or equal to the supply voltage. When the sum is greater than the power supply, both NMOS and PMOS transistors cannot be turned on at the same time and the inverter will show a schmitt-trigger like hysteresis in the transfer curve. This behavior had been reported for SiC CMOS digital circuits before in [3]. The same hysteresis is also observed in this process for the 3- and 5-μm CMOS operating on a 5 V power supply. For the 0.8-μm PMOS, it will operate in the punchthrough regime and its subthreshold drain current will increase rapidly with the drain bias even though $|V_{\rm GS}|$ is at a low value. The subthreshold current in the inverter is sufficient to drive the output load to high at a very small power supply. It is noted that there is little hysteresis in the transfer curve at various supply voltages. The high subthreshold current also produces a very gradual change from hi-to-lo transitions. At a $V_{\rm DD}$ of 5 V, the noise margins measured at the unit gain points of the voltage transfer curve are 0.3 V for NM_L and 2.5 V for NM_H, respectively. The transfer characteristic is asymmetric and has a very low value of NM_L. For desirable equal noise margins, the gate-threshold voltage should be adjusted to approximately half $V_{\rm DD}$ and this can be achieved by increasing the ratio of widths of the NMOS transistor to PMOS transistor.

Fig. 9 indicates that the maximum drain current occurs during switching, as expected. However, when the output of the inverter is driven to 0 V with an input high, the PMOS source/drain will enter punchthrough, which causes a large drain current to flow between the supply voltage and ground. Having circuits that consumed DC current is not desirable. The DC current can be eliminated by employing PMOS transistors with the anti-punchthrough implant.

Eleven-stage ring oscillators comprised of serially cascaded inverters having the same size as the inverter in Fig. 9 were fabricated to determine the operation speed. The output of the ring oscillator is buffered with a large NMOS push-pull buffer ($W_n/L_n = 240/0.8$ μm) to drive an output load capacitance of 10 pF. Output waveforms at supply voltages of 2 and 10 V are shown in Fig. 10(a). The output voltage is limited to a small amplitude due to the additional loading of the oscilloscope probe which is approximately 1 MΩ.

The supply voltage dependence on the oscillation frequency is shown in Fig. 10(b). In [3], the overlap capacitance was the primary reason for slow circuit speeds. To determine the influence of overlap on the circuit performance, transistors with 0.8- and 3-μm gate and source/drain overlaps are configured to form two different ring oscillators for comparison. The results indicate that there is a weak dependence on the overlap capacitance and the degradation is less than 43% at the high-frequency end. In this CMOS process, the dominant component that greatly affects the dynamic performance is the excessive p-type polysilicon interconnection which provides a large capacitance at the output of each stage. According to Hspice simulations, in which transistor models corresponding to the 0.8-μm NMOS and PMOS were used, a load capacitance of about 1 pF in each stage will yield an oscillation frequency matching the measured results. The maximum oscillation frequency obtained is about 1.43 MHz at 10 V, corresponding to a 31 ns gate delay per inverter stage. Compared to the

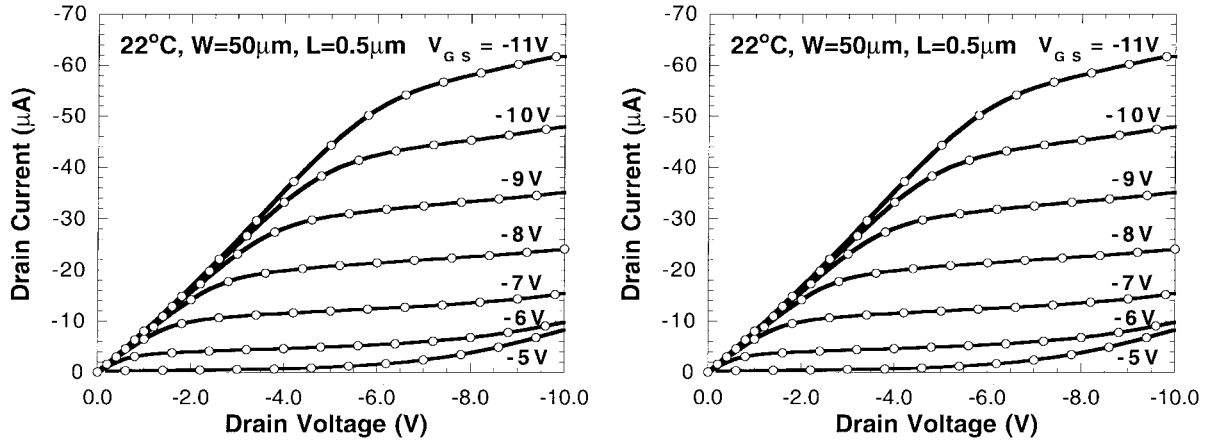


Fig. 6. Shown are the $I-V$ characteristics of (a) an 0.8-μm and (b) an 0.5-μm PMOS transistors with punchthrough stopper at room temperature.

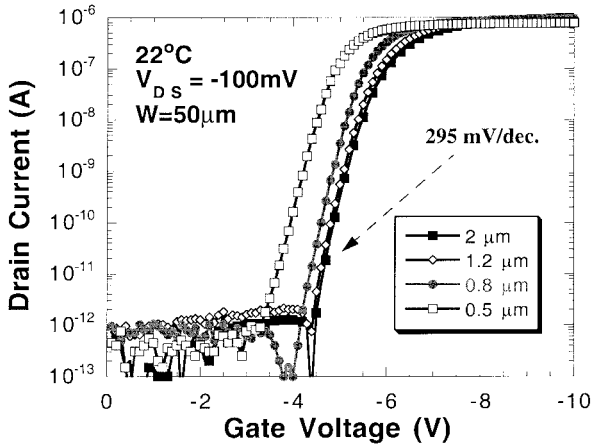


Fig. 7. Subthreshold characteristics of PMOS transistors with punchthrough stopper.

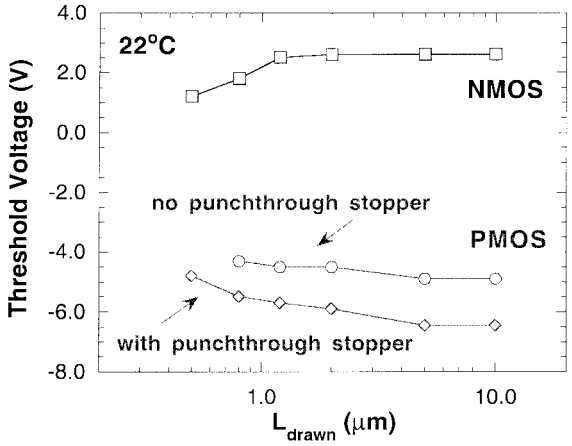


Fig. 8. Threshold voltage rolloff versus the channel length for NMOS and PMOS transistors at room temperature.

circuit speeds reported in [3], digital circuits implemented with this 0.8-μm features exhibit considerably better performance. Various logic gates have also been fabricated. Fig. 11 shows the schematics and waveforms for an EXNOR/EXOR gate measured at room temperature. It should be noted that the EXNOR/EXOR gate has fast rise and fall times. This is because the circuit employs cross-coupled PMOS transistors which form a differential latching circuit while the logic is performed by complementary NMOS arrays. This scheme is used to provide gain and increase the switching speed of the circuit. Since the SiC PMOS transistors have poor driving capability due to the parasitic resistance and low channel mobility, circuit techniques which are NMOS rich are required to provide significantly better performance compared to conventional static CMOS.

C. Parasitic Series Resistance Effect

The sheet resistance and contact resistance for n^+ and espe- cially, p^+ source/drain are consid- erably high in SiC. As the channel length becomes shorter, the parasitic S/D resistance becomes a significant portion of the total device resistance. The impact of this series resistance must be accounted for in the device design so that the benefits of scaling of the device channel lengths are maximized.

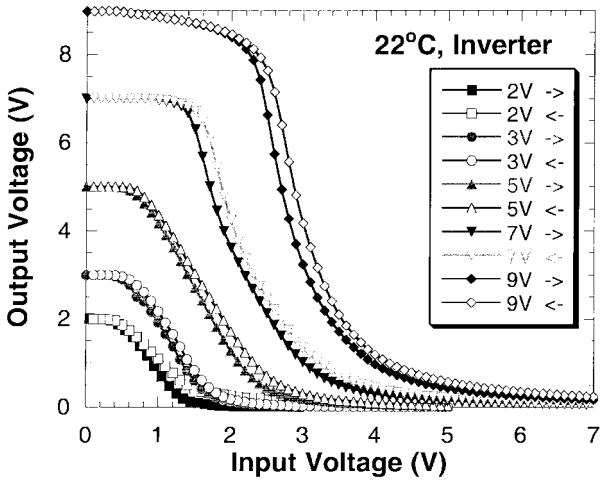
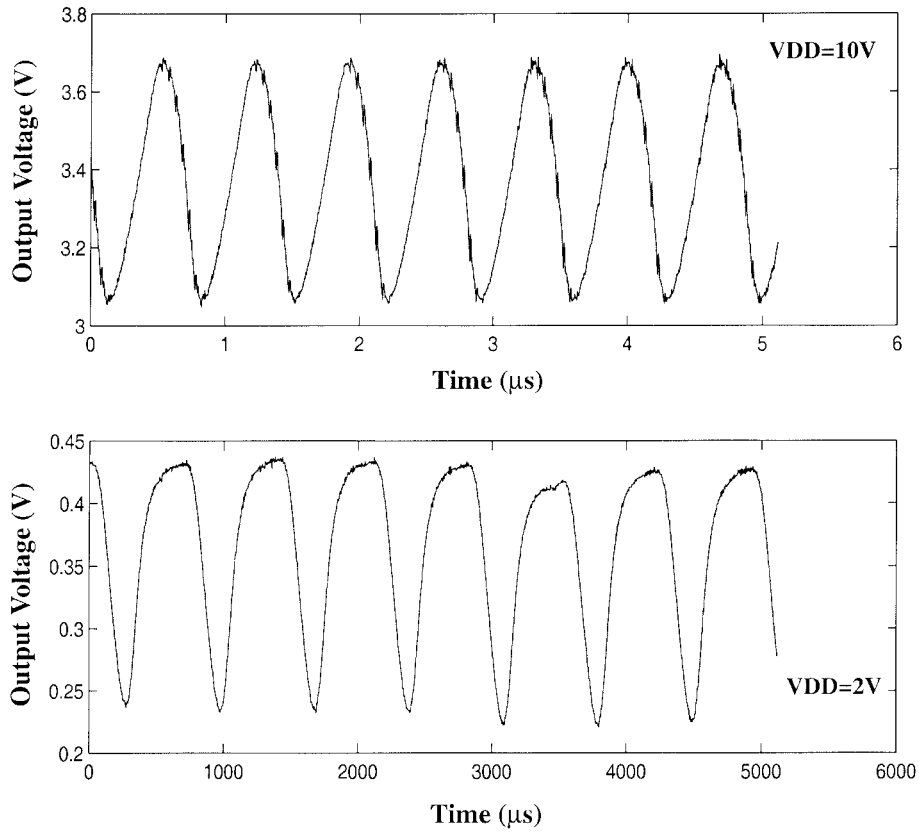


Fig. 9. Voltage transfer curves of an inverter with $W_p/L_p = 30/0.8$ μm and $W_n/L_n = 10/0.81$ um. Supply voltage ranges from 2 to 9 V. The supply current shown is for the transfer curve switching at $V_{\rm DD} = 9$ V.

The peak transconductance in the saturated region $g_{m(\rm sat)}$ at $|V_{\rm DS}| = 5$ V for both NMOS and PMOS transistors are plotted in Fig. 12 as a function of effective channel lengths. Fig. 12(a) includes the transconductance of LDD-type NMOS



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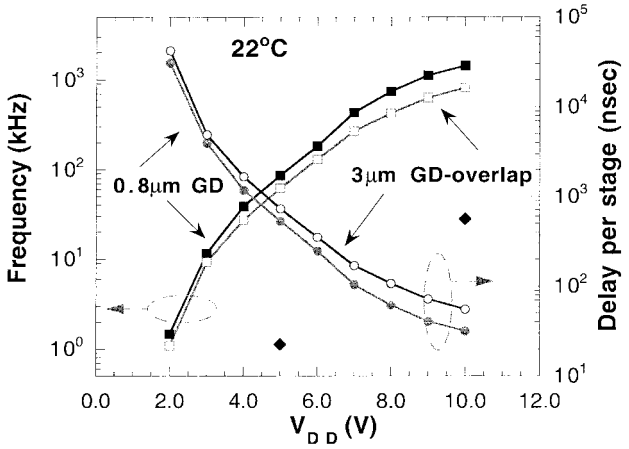

(b)

Fig. 10. (a) Output waveforms of an 11-stage ring oscillator operating at $V_{\rm DD} = 10$ V and $V_{\rm DD} = 2$ V. The size of each inverter stage is the same as that of the inverter in Fig. 9. (b) Measured oscillation frequency and delay per stage of the ring oscillator versus supply voltage. The symbol (μ) in the figure is for the oscillation frequency of the 5-μm CMOS ring oscillator fabricated in [3].

devices, which were fabricated by adding one more mask level for the n^- implant. The key parameters for the LDD NMOS are presented in Table I. The n^- region between the channel and the source/drain is about 0.3 μm. This region is used to lower the peak electric field at the drain and body junction, thus reduce the depletion width into the channel and allow a higher bias to be applied at the drain with less short-channel effects. Short-channel devices with this structure have shown better saturation characteristics. However, the LDD region will introduce a high series resistance into the device. In this discussion, we are interested in the effect of its parasitic resistance on the scaling of channel length.

The solid lines in Fig. 12 are power law fits of the measured data, which are presented as symbols. Note that there is no limitation for the NMOS transconductance to increase as $L_{\rm eff}$ is scaled into the 0.3-μm regime. The transconductance of LDD NMOS shows a weaker dependence than for the conventional NMOS transistor at room temperature. As the series resistance decreases at 300 °C, its degradation effect on the transconductance is reduced and the power coefficient becomes approaching -1.

For PMOS transistors, the increase of transconductance with

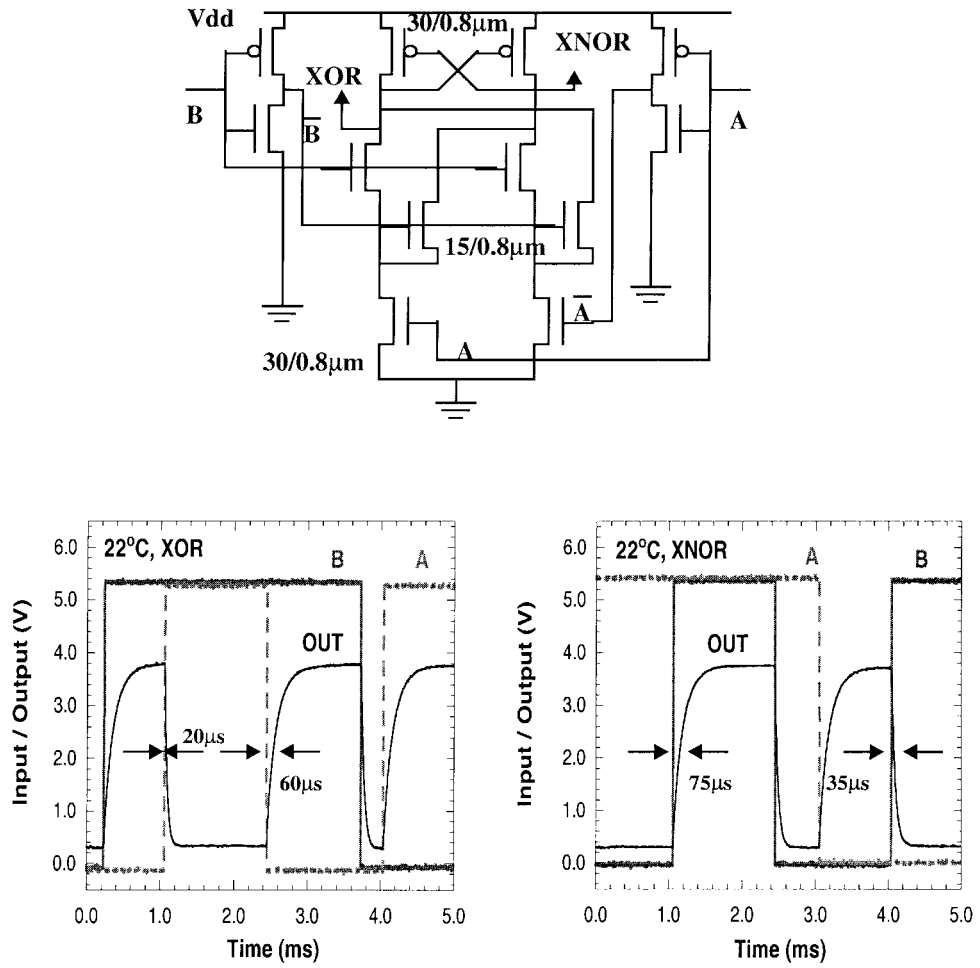

Fig. 11. Schematic and output waveforms for an XOR/XNOR gate with $V_{\rm DD} = 5$ V.

$L_{\rm eff}$ at room temperature is retarded by the parasitic series resistance. As the temperature is increased to 300 °C, the p^+ sheet resistivity and specific contact resistivity are significantly reduced to 4.2 kΩ/sq. and 3.3×10^{-3};Ω-cm^2, respectively. The relation of $g_{m(\rm sat)}$ and $L_{\rm eff}$ has changed from $\sim L^{-0.1}$ to $\sim L^{-0.52}$ accordingly. Compared to the NMOS, PMOS transistors show a very slow increase of $g_{m(\rm sat)}$ with scaled $L_{\rm eff}$.

For NMOS transistors, the scaling of channel length is a very effective way to improve the current driving capability because the source/drain parasitic resistance is lower than the channel resistance. As the n-channel mobility continues to be improved by oxidation processes [13], the channel resistance will be reduced and the dependence of $L_{\rm eff}$ on $g_{m(\rm sat)}$ will change. Whether the transconductance will increase as $\sim L_{\rm eff}^{-1}$ with the improvement of the channel mobility is still an open question.

For PMOS transistors, the source/drain series resistance is the dominant component and driving current can only be increased by reducing parasitic series resistance. This can be seen from the increase of the power coefficient in $L_{\rm eff}$ at a high temperature as the series resistance is significantly reduced. One possible solution is to reduce the spacing between the contact and channel by the formation of a self-aligned silicide (or salicide). The silicide sheet resistance would be more attractive than the diffusion sheet resistance because there is no carrier freeze-out problem of Al at room temperature. As the sheet resistance is lowered, the source and drain series resistance can only be benefited by the improvement of contact materials on the p^+ region.

TABLE I
KEY PARAMETERS FOR LDD NMOSFET

Parameter	22°C	300°C
Gate oxide thickness	260 Å	
p-epilayer doping	2.1×10^{17} cm^{-3}	
long channel NMOS V_T	4.1 V	2.8 V
N+ sheet resistivity	2.7 kΩ/sq.	1.36 kΩ/sq.
N- sheet resistivity	13.8 kΩ/sq.	6.7 kΩ/sq.
channel mobility	10.5 cm^2/V-s	14.9 cm^2/V-s
ΔL (= L_{drawn} - L_{eff})	0.10 μm	0.15 μm

IV. SUMMARY AND CONCLUSIONS

In conclusion, this work demonstrated that CMOS devices and digital circuits in 6H-SiC have been fabricated using gate lengths in submicron regime, with effective punchthrough control. NMOS transistors have shown increased driving ca-

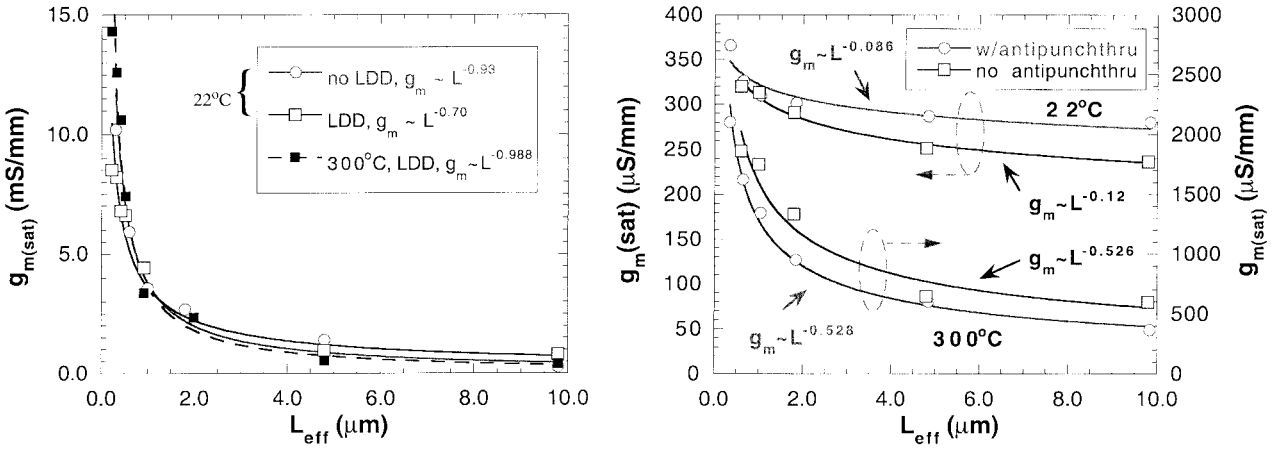

Fig. 12. (a) Measured peak saturated transconductance versus effective channel length for (a) NMOS transistors and (b) PMOS transistors at room temperature and 300 °C.

pability and good subthreshold characteristics down to 0.5 μm. PMOS transistors in this process are more susceptible to punchthrough because they are fabricated on a very lightly doped n-epilayer. A 0.5-μm PMOS transistor will operate only in punchthrough if no precautions are taken to engineer the channel. A channel implant (B and N) for PMOS has been used to suppress punchthrough while adjusting the threshold voltage to a reasonable value. No significant degradation of channel mobility has been observed after this implant. CMOS digital logic circuits with 0.8-μm channel lengths operate at faster speeds than previously reported results. Inverters and ring oscillators can operate with some short-channel effects under a 2 V power supply. This is believed to be the lowest supply voltage having been demonstrated on SiC circuits.

As the channel is scaled, the core issue of improving the device intrinsic performance will move from engineering the channel to that of reducing the parasitic source-drain resistance. The effect of parasitic resistance has been studied. This source-drain resistance becomes more important for PMOS transistors as it dominates the channel resistance. To make the scaling technology benefit SiC CMOS performance, future directions should investigate the formation of p^+ region with high concentration and low contact resistivity.

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REFERENCES

[1] D. B. Slater, Jr., G. M. Johnson, L. A. Lipkin, A. V. Suvorov, and J. W. Palmour, "Demonstration of a 6H-SiC CMOS technology," in *IEEE Device Res. Conf. Dig.*, Santa Barbara, CA, June 24–26, 1996, pp. 162–163.

[2] S. Ryu, K. T. Kornegay, J. A. Cooper, Jr., and M. R. Melloch, "Monolithic digital CMOS integrated circuits in 6H-SiC using an implanted p-well process," *IEEE Electron Device Lett.*, vol. 18, pp. 194–196, May 1997.

[3] S. Ryu, K. T. Kornegay, J. A. Cooper, Jr., and M. R. Melloch, "Digital CMOS IC's in 6H-SiC operating on a 5 V power supply," *IEEE Trans. Electron Devices*, vol. 45, pp. 45–53, Jan. 1998.

[4] J. N. Shenoy, J. A. Cooper, Jr., and M. R. Melloch, "High-voltage double-implanted power MOSFET's in 6H-SiC," *IEEE Electron Device Lett.*, vol. 18, pp. 93–95, Mar. 1997.

[5] J. Spitz, M. R. Melloch, J. A. Cooper, Jr., and M. A. Capano, "2.6 kV 4H-SiC lateral DMOS- FET's," *IEEE Electron Devices Lett.*, vol. 19, pp. 100–102, Apr. 1998.

[6] W. Xie, J. A. Cooper, Jr. and M. R. Melloch, "Monolithic NMOS digital integrated circuits in 6H-SiC," *IEEE Electron Device Lett.*, vol. 15, pp. 455–457, Nov. 1994.

[7] J.-S. Chen and K. T. Kornegay, "A class AB SiC CMOS power OPAMP with stable voltage gain over a wide temperature range," *Proc. Inst. Elect. Eng.—Circuits, Devices and Systems*, vol. 144, pp. 22–28, Feb. 1997.

[8] J. Chen, S. Ryu and K. T. Kornegay, "A silicon carbide CMOS intelligent gate driver circuit," *IEEE J. Solid State Circuits*, vol. 34, pp. 192–204, Feb. 1999.

[9] B. J. Baliga, "An overview of smart power technology," *IEEE Trans. Electron Devices*, vol. 38, pp. 1568–1575, July 1991.

[10] S. Seshadri, A. K. Agarwal, L. B. Rowland, J. B. Casady, and C. D. Braudt, "Demonstration of a 700 V asymmetrical, 4H-SiC gate turn-off thyristor (GTO)," in *IEEE Device Res. Conf.*, Fort Collins, CO, 1997.

[11] K. Terada and H. Muta, "A new method to determine effective MOSFET channel length," *Jpn. J. Appl. Phys.*, p. 953, May 1979.

[12] J. G. Chern, P. Cheang, R. F. Motta, and A. Godinho, "A new method to determine MOSFET channel length," *IEEE Electron. Device Lett.*, vol. 1, pp. 170–173, Sept. 1980.

[13] L. A. Lipkin and J. W. Palmour, "Improved oxidation procedures for reduced SiO_2/SiC defects," *J. Electron Mater.*, vol. 25, no. 5, pp. 909–915.

[14] J. N. Shenoy, G. L. Chindalore, M. R. Melloch, J. A. Cooper, Jr., J. W. Palmour and K. G. Irvine, "Characterization and optimization of the SiO_2/SiC MOS interface," *J. Electron. Mater.*, vol. 24, pp. 203–209, 1995.

[15] T. Kimoto, A. Itoh, H. Matsunami, T. Nakato and M. Watanable, "Aluminum and boron ion implantation into 6H-SiC epilayers," *J. Electron. Mater.*, vol. 25, no. 5, pp. 879–884, 1996.

[16] ———, "The effects of n^+ dose in implantation into 6H-SiC epilayers," *J. Electron. Mater.*, vol. 24, no. 4, pp. 235–240, 1995.

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